DATA SHEET
HSCDTD015A

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History of revision

Datasheet Rev.	Date	Page	Note
1.0	27.Jun.2025		First edition
1.1	28.Nov.2025	P32	Add recommended soldering conditions.
			Add Reel and Tape informations.
		P33	Add Reel and Tape informations.

OVERVIEW

HSCDTD series is three axis terrestrial magnetism sensor of the digital output.
A high sensitivity magnetic sensor that detects the terrestrial magnetism element is mounted.
It provides with the drive circuit, the signal processing circuit, and the serial interface.

FEATURES

- 3-Axis magnetic sensor with (XYZ) 0.075 [μT/LSB] resolution
- Output, x, y, z axis magnetic field strength.
- Serial interface
  I2C slave interface (SS、FS、FS+) PhilipsI2C revision .2.1 and
  NXP UM10204 I2C-bus specifications and user manual Rev.03-19 June 2007 is supported.
-16 pin, FLGA package
- Package size : 1.6×1.6 x t0.64mm (Maximum size)
- Low current consumption
- Lead free, RoHS instruction, Halogen free conforming

- Function
  - Initialization Function (Power on reset)
  - Functional Mode
    Standby Mode
    Continuous Measurement Mode (CMM)
    (Data Rate 10 / 50 / 100 / 200Hz Selectable)
    One-shot Mode
  - Temperature Compensation Function
  - Data Ready Function
  - Interrupt Function
  - FIFO Function

- Supply Voltage
  - Analog 1.6 to 2.0 V
  - Digital 1.14 to 2.0 V

- Operating Temperature -40 to +85°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Maximum voltage supply(AVDD/VDDIO)	Vmax	-0.5		3.6	V
Storage Temperature	Tstg	-40		+125	℃
Electrostatic discharge protection @ HBM		1500			V
Electrostatic discharge protection @ CDM		350			V

ELECTRICAL CHARACTERISTICS

Temperature condition : 25 degC

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage AVDD		AVDD	1.6		2.0	V
Supply Voltage DVDD		VDDIO	1.14		2.0	V
Standby Mode current		IDAstb		19	40	μA
One shot mode current		IDAosm		21	45	μA
CMM Average current consumption @ 50Hz±10% @AVDD=1.8V	TAP=6bit	IDAlp_avg		84		μA
	TAP=7bit			121		
	TAP=8bit			196		
	TAP=9bit			344		
CMM Average current consumption @ 100Hz±10% @AVDD=1.8V	TAP=6bit	IDAlp_avg		146		μA
	TAP=7bit			222		
	TAP=8bit			369		
	TAP=9bit			666		
CMM Average current consumption @ 200Hz±10% @AVDD=1.8V	TAP=6bit	IDAlp_avg		273		μA
	TAP=7bit			420		
	TAP=8bit			717		
	TAP=9bit			1311		
Digital IO Low Level Input Voltage		VIL	-0.5		VDDIO*0.3	V
Digital IO High Level Input Voltage		VIH	VDDIO*0.7		VDDIO+0.5	V
Digital IO Low Level Output Voltage		VOL	-0.5		VDDIO*0.3	V
Digital IO High Level Output Voltage		VOH	VDDIO*0.7		VDDIO	V
I2C Clock Frequency	Standard/Fast+	I2Cffs	0.1	0.4	1	MHz
SPI Clock Frequency @ VDDIO=1.8V		SPIf		12	20	MHz
TRG pull-down resistance	VDDIO = 1.14 V	R_{TRG}	230	373	570	kohm
	VDDIO = 1.8 V		70	114	180	
	VDDIO = 2.0 V		50	94	150	
TRG input pulse width (active high)		PW_{TRG}	20			μsec
INT pull-up resistance (Open-drain setting only)	VDDIO = 1.14 V	R_{INT}	167	266	401	kohm
	VDDIO = 1.8 V		64	98	145	
	VDDIO = 2.0 V		55	83	122	

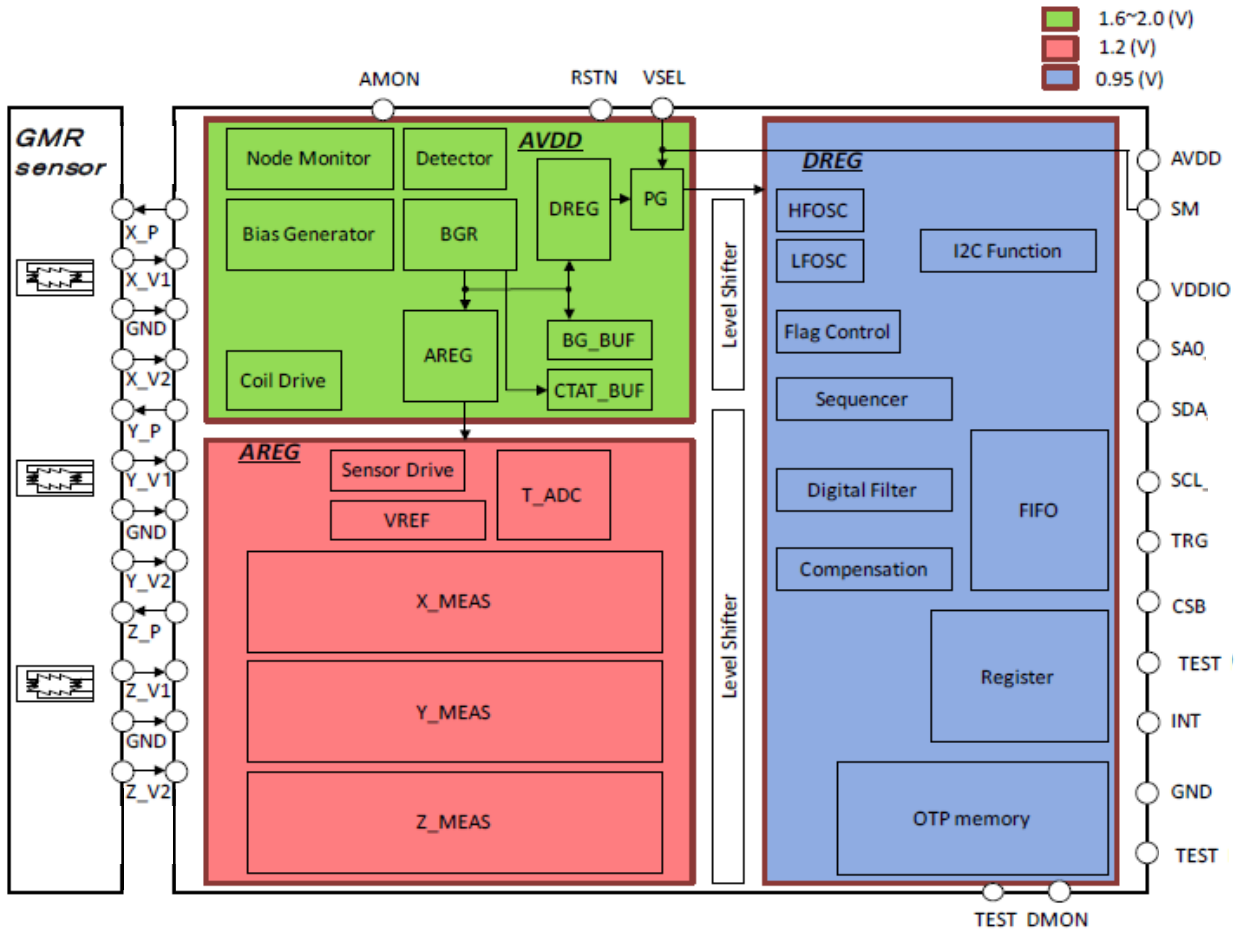
MAGNETIC CHARACTERISTICS

Temperature condition : 25 degC

Characteristics			Symbol	Min.	Typ.	Max.	Unit
Operating Temperature			Ta	-40		+85	℃
Full Scale Range, Magnetic field measuement			FSmag	-2.4		+2.4	mT
Sensitivity Error			Smag,err	-2.5		2.5	%
Resolution			Res	0.073	0.075	0.077	μT/LSB
Temperature Resolution			TPres		0.03125		°C/LSB
RMS Noise	CMM TAP=7bit	X	Nmag,rms		0.09	0.17(※1)	μT
		Y			0.10	0.17(※1)	
		Z			0.11	0.17(※1)	
	CMM TAP=8bit	X			0.08		
		Y			0.09		
		Z			0.10		
	CMM TAP=9bit	X			0.07		
		Y			0.08		
		Z			0.09		
Output Data Rate		ODR=00 ODR=01 ODR=10 ODR=11	ODRmag		200 100 50 10		Hz
CMM Meas Time		TAP=6bit TAP=7bit TAP=8bit TAP=9bit	MTlpm		0.310 0.502 0.886 1.654		msec
Temperature Measurement Time		TAP=5bit	MTts		126		μsec
		TAP=6bit			174		μsec
Software Reset Time			Tsrst		165	180	μsec
Zero-field Offset Variation over Temperature			ΔOSmag,t	-0.1		0.1	μT/°C
Sensitivity Error over Temperature			Smag,err,t	0.0		2.5	%
Sensitivity Error Mismatch between axes			Smag,err,mis	-1.0		1.0	%
Nonlinearity			Lmag	0.0		2.0	%
Hysteresis @ ±1.2mT			Hys			2.0	uT

(※1) Noise inspection is performed with TAP=7 bit only and Max value is inspection Spec.

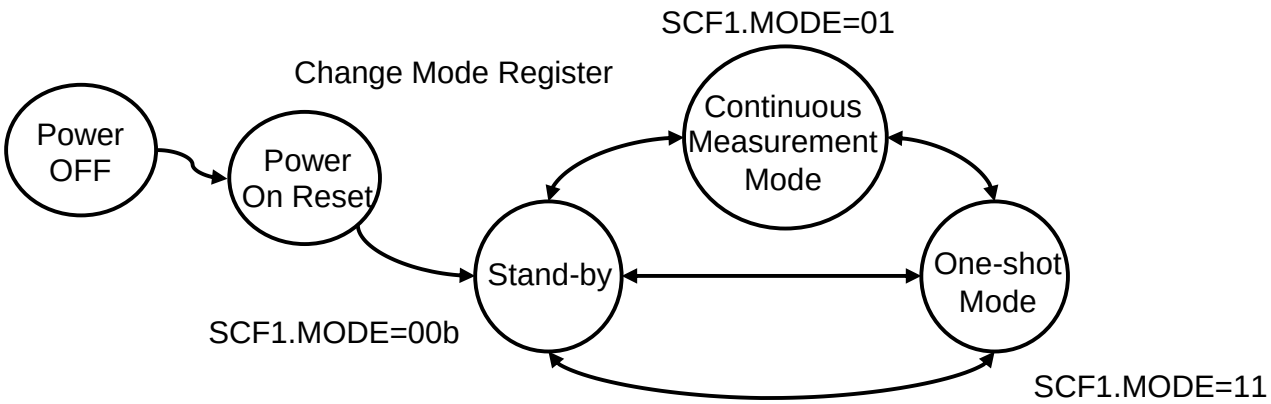
BLOCK DIAGRAM



FUNCTIONAL SPECIFICATIONS

Function List

Name	Description
Initialization	Power on reset is performed by turning on the power. All circuits and registers are set to default and mode is set to Standby Mode automatically by POR. Software reset is performed by writing to control register. All register except OTP register is set initial value.
Functional Modes	This sensor has Standby Mode and active mode for power control. There are 2 states in active mode.
Off mode	The sensor is not active when AVDD or VDDIO is disable.
Standby Mode	Low power waiting state. Standby Mode can access to register.
Active Mode	Change from Standby Mode to active mode by register command to Sensor Config1 register.
Continuous Measurement Mode (CMM)	Continuous interval measurement. Interval time depends on ODR setting.
One-shot Mode (OSM)	External Trigger Measurement / Register Action Measrurement Measruemet is same as CMM setting
Interrupt Function	Measurement event
Data Ready function	Informs when new measured results are updated. It is possible that data ready inform the signal to the DRDY pin when updated output data.
FIFO Threshold function	Informs when FCNT is greater than or equal to FFTH.
FIFO Full function	Informs when all 64 data are stored in the FIFO.
POR event function	Informs when POR is completed.
SRST event function	Informs when SRST is completed.
Temperature Measurement Function	Retrieve temperature data from internal temperature sensor. Temperature data is used for internal compensation for output data.
Temperature Compensation Function	Compensate gain and offset in digital circuit by temperature measurement results.



State Machine

FUNCTIONAL SPECIFICATIONS (Continued)

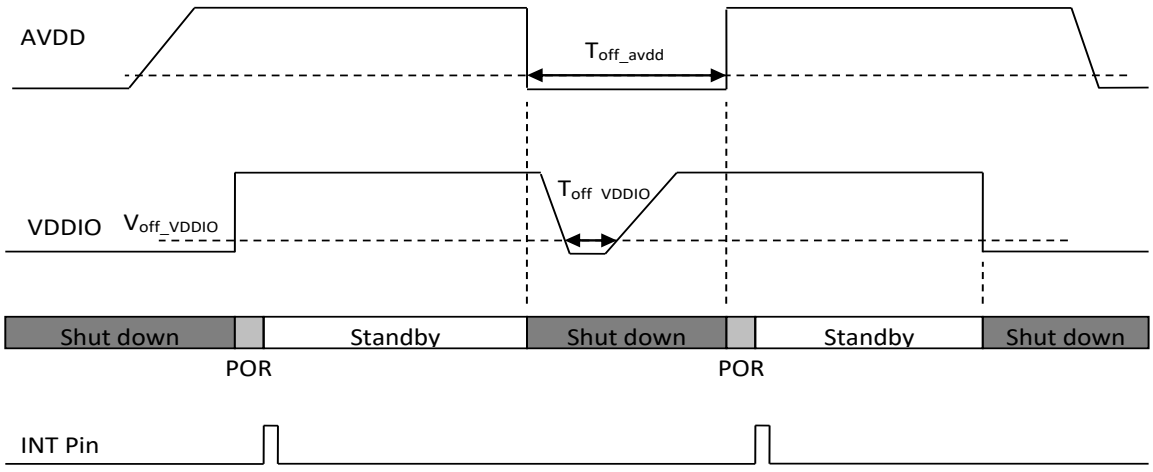
Initialization

- All internal circuits and all register values are initialized with POR (Power On Reset) after power-on.
- After initialization, the functional mode move to Standby Mode automatically.
- The software reset set by the register command /CCF.SRST=1 makes all register value to defaults.

Supply Power Specifications

Supply power sequence

- Supply power sequence for AVDD and VDDIO shall not be limited.
  However, Ramp Time shall be satisfied 0.01 ~ 3 ms at the 10% ~ 90% range of the voltage.
- Reset is extended for 192 clocks of LFOSC count after detection of AVDD and VDDIO voltage.
  And then, it shall release the Reset if AVDD voltage and VDDIO are available.
- Supply power sequence read OTP after Reset release, and output pulse signal from INT pin,
  and then transit to Standby Mode.



Power ON/OFF Sequence

Shut-down specifications

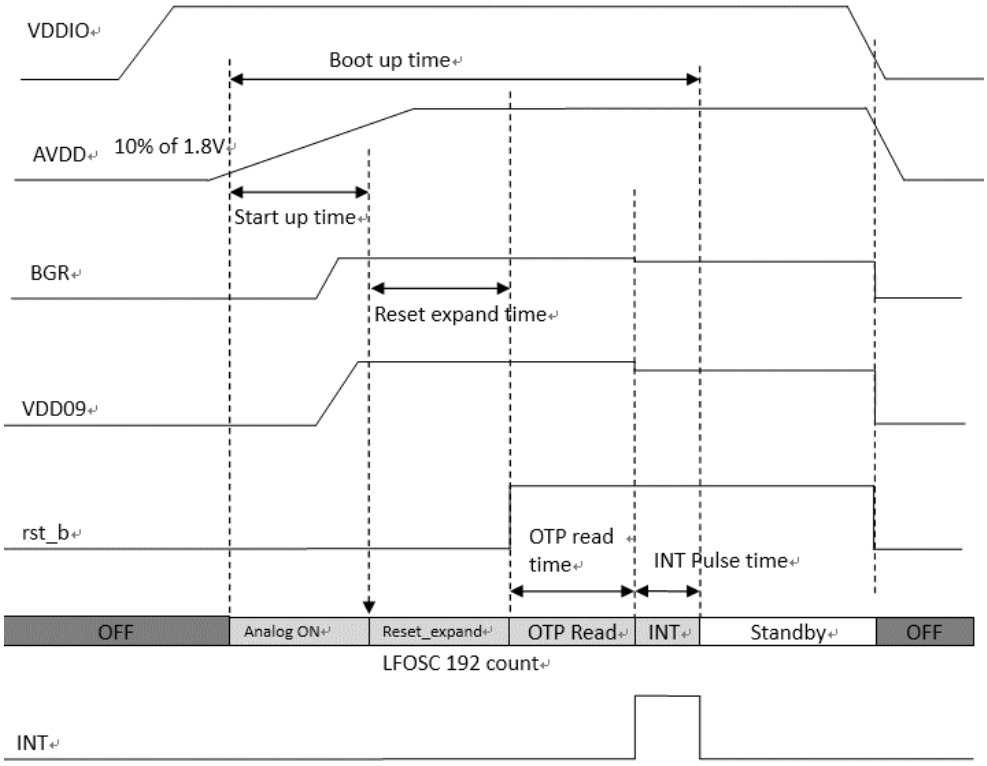
Parameters	Symbols	Conditions	Characteristics			Units
			MIN	TYP	MAX	
AVDD Shut Off voltage	V_{off_AVDD}		0		0.3	V
VDDIO Shut Off voltage	V_{off_VDDIO}		0		0.3	V
AVDD Shut Off time	T_{off_AVDD}		0.1			msec
VDDIO Shut Off time	T_{off_VDDIO}		0.1			msec

FUNCTIONAL SPECIFICATIONS (Continued)

Supply Power Specifications (Continued)

Power operation

- Power Operation detects power line voltage in ASIC after AVDD and VDDIO were supplied, and make LFOSC work, and extend Reset 192 clock.
- Power Operation reads OTP after Reset extension, then transit to Standby Mode. It shall not allow the access by I/F during this operation.



Power On Sequence

Power On Sequence Specifications

Parameters	Symbols	Conditions	Characteristics			Units
			MIN	TYP	MAX	
Power rise time	T_{Prise}	10& - 90%	0.01		3	msec
Power fall time	T_{Pfall}	10& - 90%	0.1		3	msec
Start up time	T_{start}	10% to rest release	1.4		2.2	msec
Reset_expander time	T_{rexp}		0.89		1.4	msec
OTP read 64 Byte	$T_{OTPread}$			100	200	usec
INT pulse time	T_{INT_POR}		148.5	165	181.5	usec
Boot-up time	T_{bootup}	From 10% of 1.8V to Standby			4	msec

FUNCTIONAL SPECIFICATIONS (Continued)

Modes

OFF mode

- The sensor is not active when AVDD or VDDIO is disable.

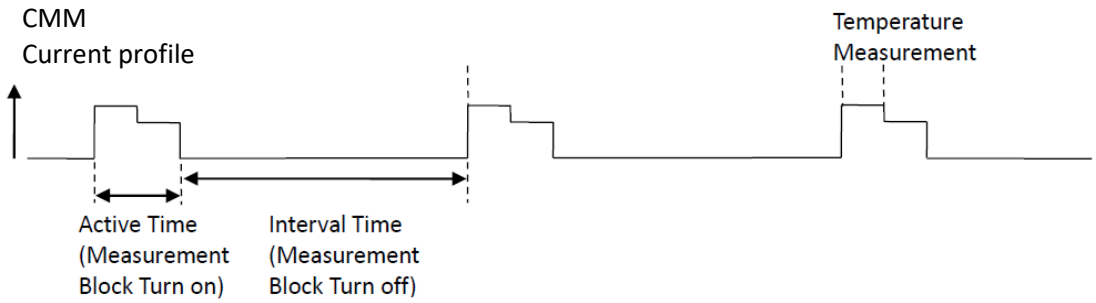
Standby Mode

- After loading the POR (Power On Reset), internal state is moved to Standby Mode automatically.
- Standby Mode is set by the register command /SCF1.MODE=00b.

Active Mode

Continuous Measurement Mode [CMM]

- Continuouse Measurement Mode is set by the register command /SCF1.MODE=01b.
- After the measurement is completed, the measurement circuit is shut down to maintain low current consumption.
- X, Y, Z axis and temperature measurement is simultaneously performed
- Measure automatically according to the set Output Data Rate (ODR).
- Temperature compensation is performed automatically by measurement with a temperature sensor.

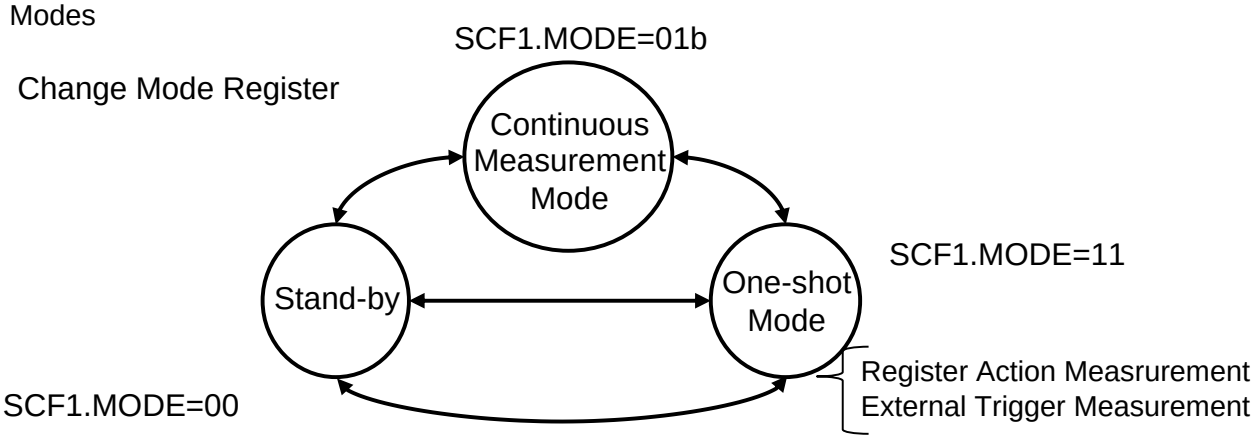


CMM Current Profile

One-shot Mode

- One-shot Mode is set by the register command /SCF1.MODE=11b.
- Register Action Measrurement is performed by accessing the register /SACT.MES=1b.
- External Trigger Measurement is performed by inputting the pulse into the TRG terminal.
- Measurement setting is the same setting as CMM.

Modes



The diagram on mode transfer

FUNCTIONAL SPECIFICATIONS (Continued)

Register configuration

Register configuration change behavior

- In case of changing register related measurement,
  the measurement shall be started with new configuration after writing completion.
- In case during measurement, analog circuit shall be reset,
  and then start measurement with new conditions.
- In case of OneShotMode, measurement shall be ended,
  and no new measurement shall be started automatically.

Register configuration behavior

Register	bit	Description	Mode	Measure	FIFO	Status	INT pin
CCF	SRST	Software Reset	All	clear	clear	clear	clear
ISO	DRDY FTHS FFUL	Data Ready FIFO Threshold FIFO Full	CMM OSM	-	-	-	clear or re-assert
FFCF	FFMD	FFMD=00b : BypassMode , FIFO, /ISTA.FFHR, /ISTA.FFUL Clear	CMM OSM	-	clear	clear FTHS & FFUL	clear or re-asser
	FFTH	FIFO Count FCNT>=FFTH : assert	CMM OSM	-	-	clear or re-assert	clear or re-assert
SCF1	TDIS RES TAP[1:0] ODR[1:0]	TEMP Disable Resolution Select Mesure TAP Output Data Rate	CMM	clear & re-start	-	-	-
			OSM	clear	-	-	-
	MODE[1:0]	Change CMM	CMM	clear & re-start	-	-	-
		MODE=11b OSM	OSM	clear	-	-	-
		MODE=00b (Stand-by)	STB	clear	clear	clear	clear

FUNCTIONAL SPECIFICATIONS (Continued)

FIFO event function (Continued)

FIFO Data

There are 64 count for FIFO and it consists of reserved 8 Bytes and TEMP 2 Bytes and MAG 6Bytes.
The reading of FIFO is done by register address 27h.

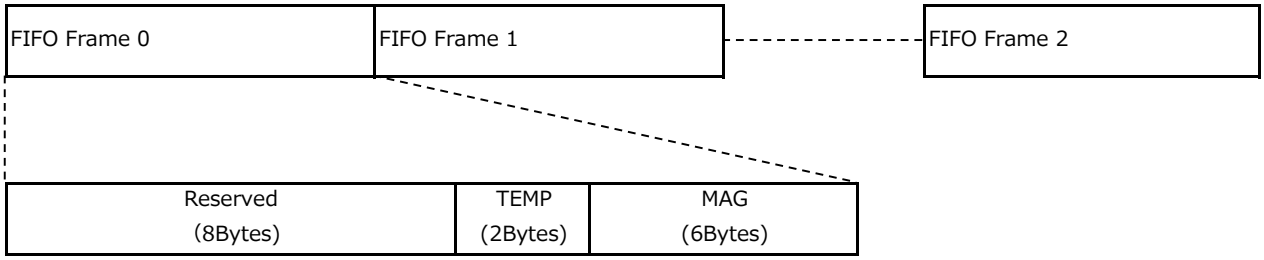


図11：FIFO Frame Description

FIFO frame description

FIFO structure

Number	Resister Name	Bit information								empty
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Byte0	Reserved	-								-
Byte1										
Byte2										
Byte3										
Byte4										
Byte5										
Byte6										
Byte7										
Byte8	Temperature Data LSB	TEMP[7:0]								7Fh
Byte9	Temperature Data MSB	TEMP[15:8]								7Fh
Byte10	X Magnetic Data LSB	MAGX[7:0]								7Fh
Byte11	X Magnetic Data MSB	MAGX[15:8]								7Fh
Byte12	Y Magnetic Data LSB	MAGY[7:0]								7Fh
Byte13	Y Magnetic Data MSB	MAGY[15:8]								7Fh
Byte14	Z Magnetic Data LSB	MAGZ[7:0]								7Fh
Byte15	Z Magnetic Data MSB	MAGZ[15:8]								7Fh

FUNCTIONAL SPECIFICATIONS (Continued)

Interrupt function

Interrupt Source

INT source list

Type	bit	Condition	Status bit
ISO.DRDY	1:selected 0:no action	INT is active High when DATA is set in DATA_REG after measurement	ISTA.DRDY
ISO.FTHS	1:selected 0:no action	INT is atctive when FIFO is over FFCF.FFTH. - FIFO_COUNT = FFTH after measurement - FIFO_COUNT ≧ FFTH after reading FIFO	ISTA.FTHS
ISO.FFUL	1:selected 0:no action	INT is active when FIFO is 64 count. - when FIFO_COUNT=63 is changed to FIFO_COUNT=64	ISTA.FFUL
POR	Always active	INT is active(pulse) after power on reset	ISTA.POR
CCF.SRST	Always active	INT is active(pulse) after software reset	ISTA.POR

Interrupt Status Clear Event

Interrupt Status Clear Condition

Status bit	Trigger	Clear Condition	Description
ISTA.DRDY	End of Meas	Read / ISTA	Read Status Byte(ADR;25h)
		Write / SCF1.MODE=00b	Change Standby Mode
ISTA.FTHS	FCNT>=FFTH	Read / ISTA	Read Status Byte(ADR;25h)
		Write / SCF1.MODE=00b	Change Standby Mode
		Write / FFCF.FFMD=00b	Change Bypass Mode
ISTA.FFUL	FCNT=63->64	Read / ISTA	Read Status Byte(ADR;25h)
		Write / SCF1.MODE=00b	Change Standby Mode
		Write / FFCF.FFMD=00b	Change Bypass Mode
ISTA.POR	End of POR/SRST	Read / ISTA	Read Status Byte(ADR;25h)

Note) Software reset : All clear, after software reset completion, ISTA.POR is asserted

FUNCTIONAL SPECIFICATIONS (Continued)

Interrupt function (Continued)

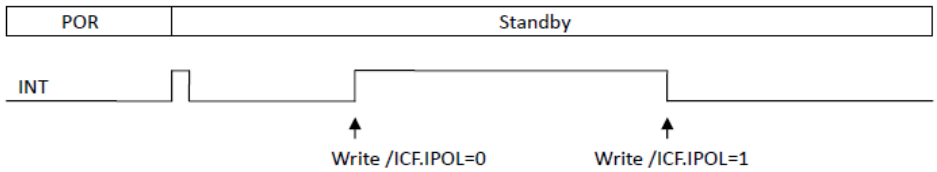
FIFO Threshold Interrupts (Continued)

Interrupt Pin Behavior

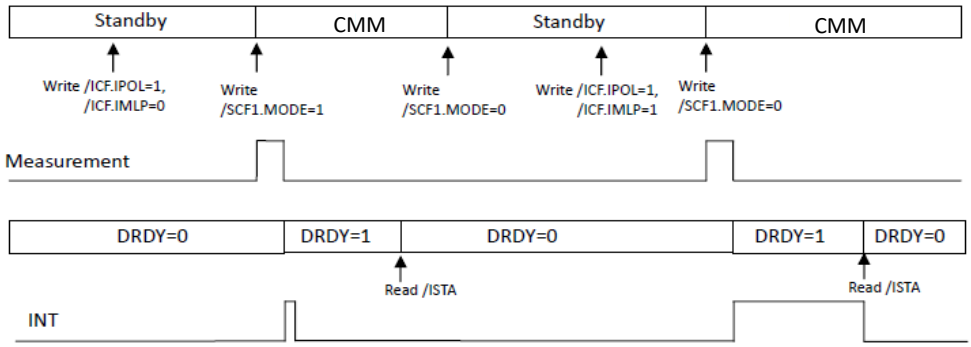
- INT Pin support Pulse Mode and Latch Mode for each interrupt function, it can be controled for each register of /ICF.
- The following table shows each condition.
- In the case of Pulse Mode, it certainly keep inactivate term after the signal activate.
- If /ICF.IPOL=1, INT Pin must Active High. If /ICF.IPOL=0, INT Pin must Active Low.
- If /ICF register was changed in CMM and OSM Mod, the function can NOT be guaranteed. /ICF should be changed in Standby Mode.

Interrupt Pin Configuration

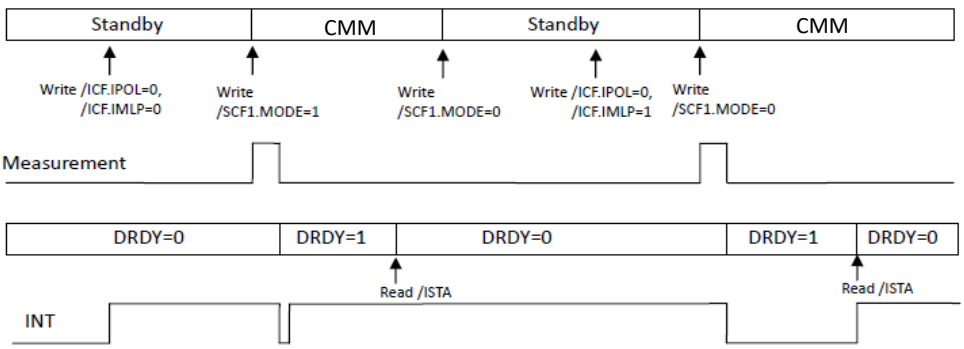
/ICF	Default	Description	bits
IMLP	0	INT Signal Mode	1: Latched Mode 0 : Pulse Mode
IPPO	1	INT PAD type configuration	1 : Push-Pull 0 : Open drain
IPOL	1	INT Signal Polarity	1 : Active High 0 : Active Low



INT polarity control on Standby Mode



INT Pulse and Latch Mode Active High



INT pulse and Latch Mode Active Low

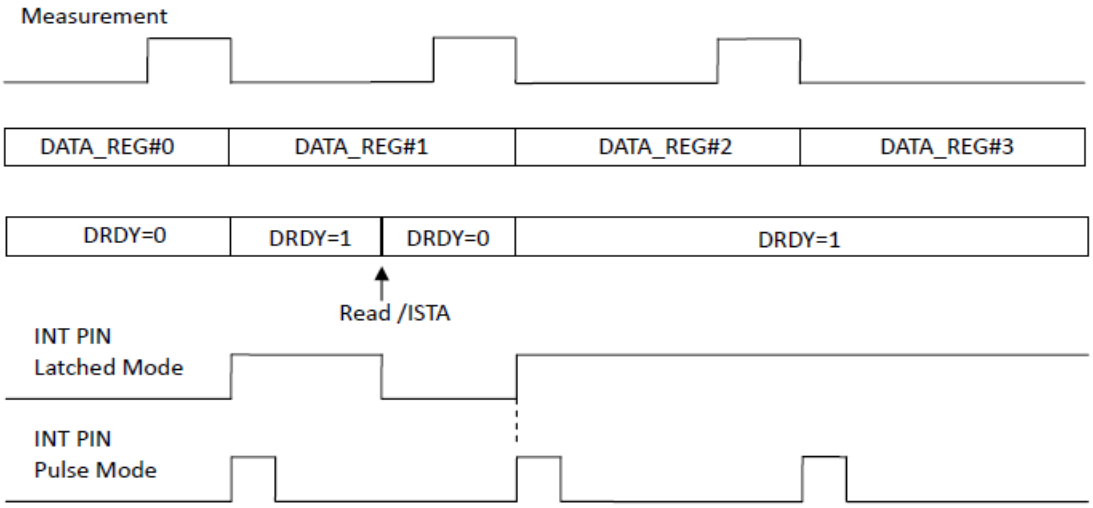
FUNCTIONAL SPECIFICATIONS (Continued)

Interrupt Function

Data ready interrupt (DRDY)

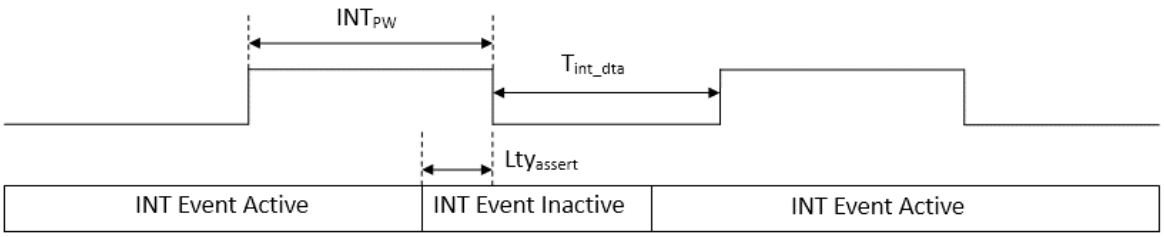
-This function is used for notice that output data was updated.

- It is possible that data ready inform the signal to the INT pin when updated output data.
- In Pulse Mode, when DATA_REG is updated, the output of the INT terminal is always output.
- In Latched Mode, as long as DRDY is not released by reading / ISTA, INT terminal keeps active state.



INT standard behavior of DRDY

Interrupt Pin Timing Specifications



INT pin specifications

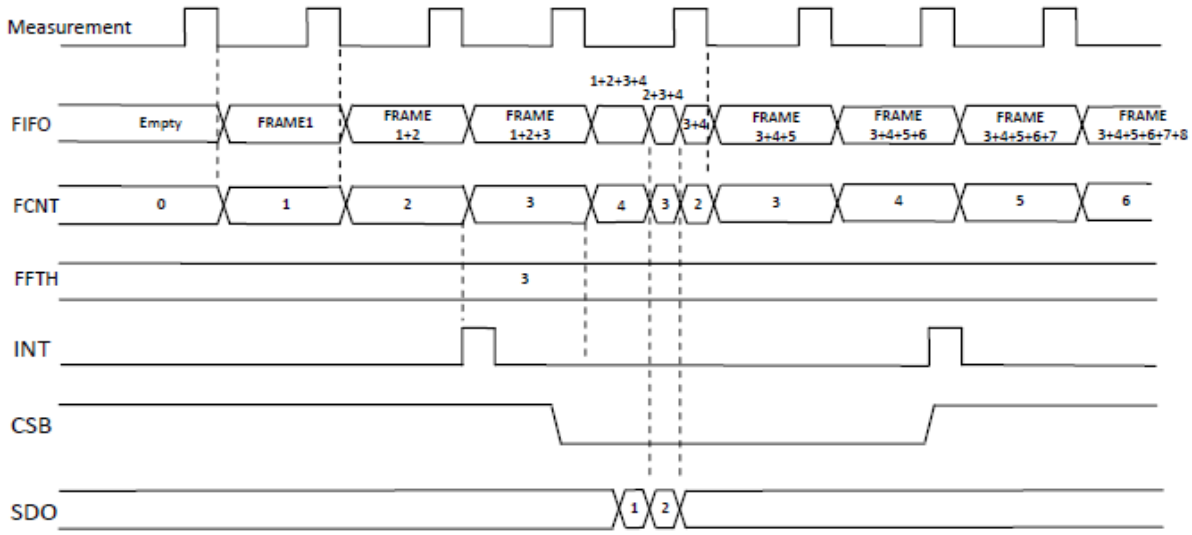
Parameter	Symbol	Characteristics			Units
		MIN	TYP	MAX	
Interrupt pulse width	INT_{PW}	148.5	165	181.5	usec
Time between interrupt de-assertion and re-assertion	T_{int_dta}	139.5	155	170.5	usec
De-assertion Latency	Lty_{assert}	0		20	usec

FUNCTIONAL SPECIFICATIONS (Continued)

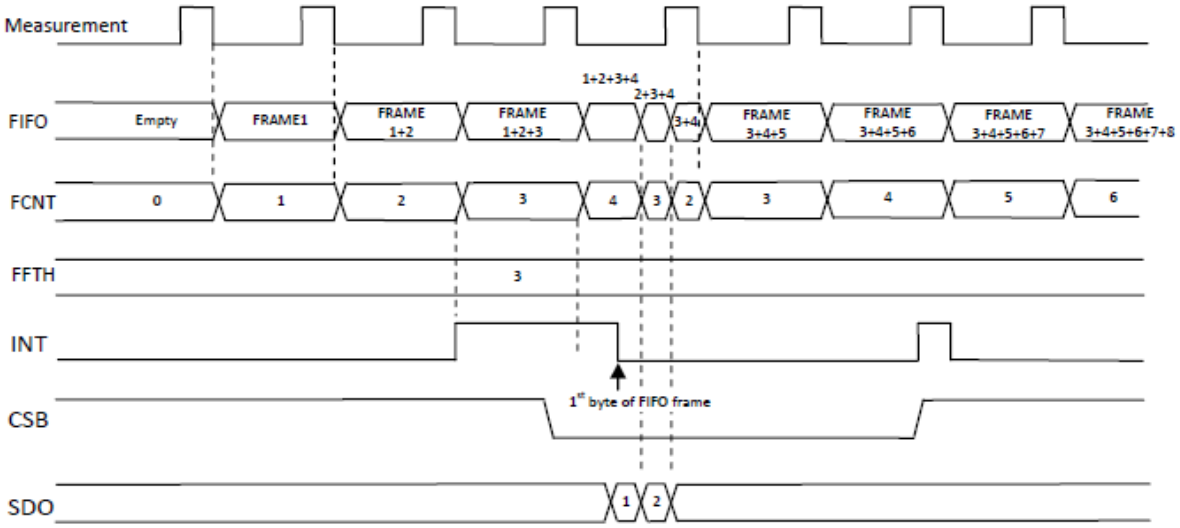
Interrupt Function (Continued)

FIFO Threshold Interrupts

- This function is used for notice that FCNT is greater than or equal to FFTH /. ISTA.FTHS = 1.
- If FCNT becomes FFTH or higher again during reading of FIFO data,
- INT signal is outputted from INT terminal at de-assertion of CSB (at the end of Read).



INT pulse mode behavior of FIFO Threshold Event



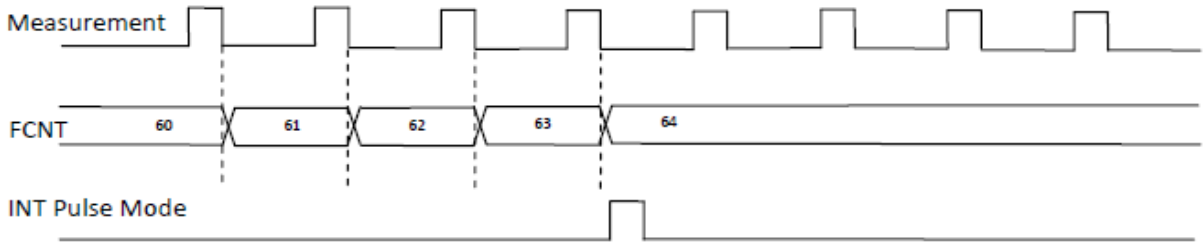
INT latch mode behavior of FIFO Threshold Event

FUNCTIONAL SPECIFICATIONS (Continued)

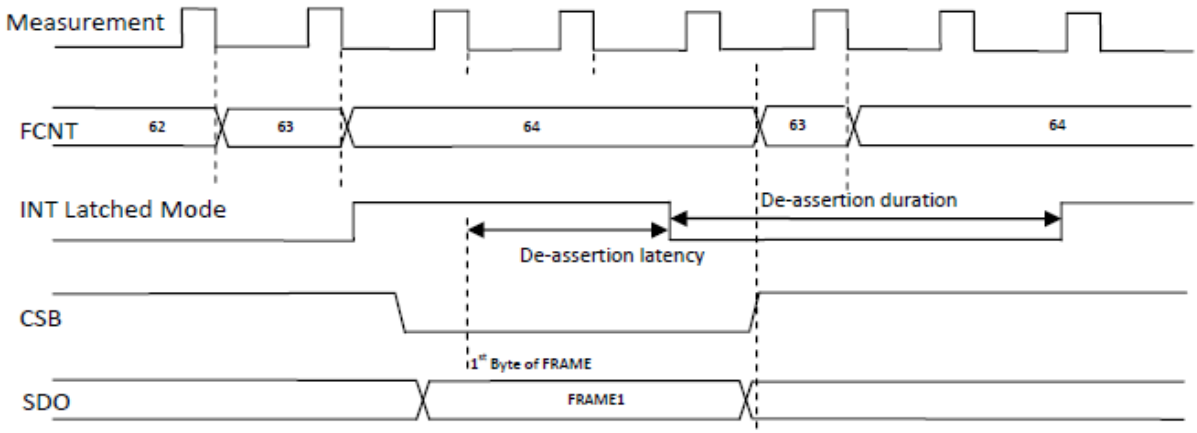
Interrupt Function (Continued)

FIFO Full Interrupts

- This function is used for notice that all 64 data are stored in the FIFO.



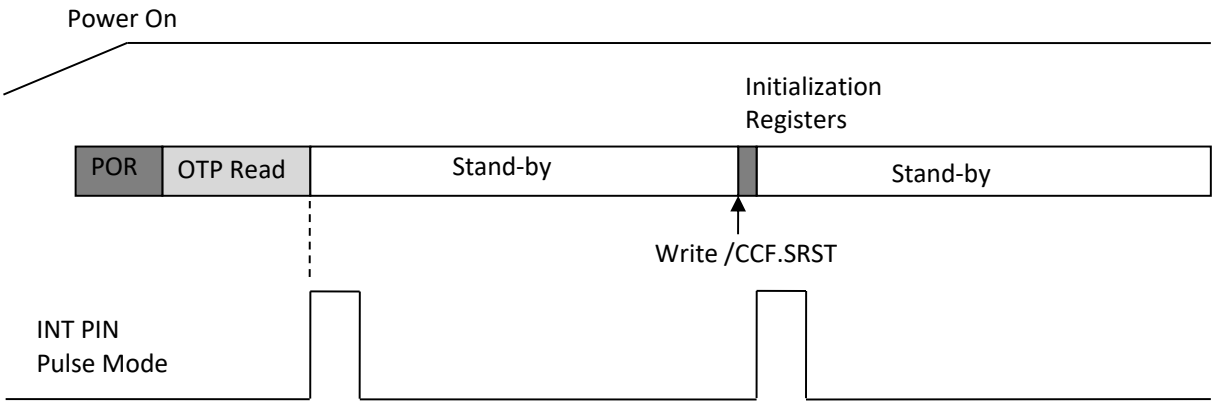
INT behavior of FIFO Full Event



INT Latched Mode behavior of FIFO Full Event

POR Interrupts / SRST Interrupts

- This function is used for notice that power-on OTP Reading or Software Reset is completed.
- Signal from INT terminal with Pulse and set / ISTA.POR = 1.

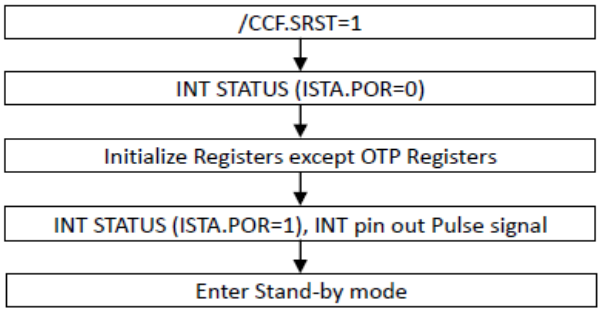


FUNCTIONAL SPECIFICATIONS (Continued)

Interrupt Function (Continued)

Software Reset

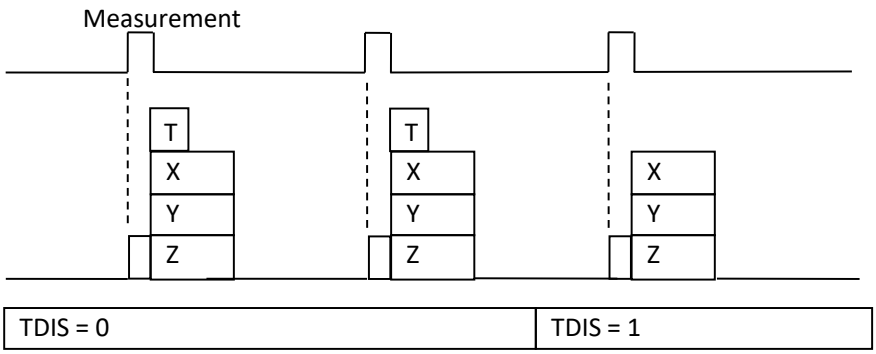
- Software reset is executed by /CCF.SRST=1.
- If software reset is executed in measurment, the measurement stops immidiately and reset is executed.
- The registers get to be default value by software reset except OTP.
- The pulse signal of reset completion is generated from INT Pin after complesion of software reset.



Software Reset Flow

Temperature Measurement

- The temperature measurement will be executed automatically together with magnetometer measurement in CMM & OSM mode, provided that SCF1/TDIS=0.
- Temperature only measurement can be executed only in TMES of One-shot Mode. And only the temperature data is updated to the FIFO, and MAGX, MAGY, MAGZ are all 7 Fh.
- When / SCF1.TDIS = 1, temperature measurement does not performed in each mode.
- When / SCF1.TDIS = 0, temperature measurement is performed simultaneously with magnetic field measurement in all modes.



TDIS (Temp Measurement Disable) Function

INTERFACE SPECIFICATIONS I2C

Interface specifications

OP53.IFS	I/F	SA0	CSB	Description
1	I2C	Input	Output(High)	2 wire I2C, Standard / Fast / Fast Plus

Register write constraints

- 71.5us interval of writing into the same configuration register
- In case of I2C, it shall be specified the time(ti2c_sptwd) from StopCondition to data write of next communication.
- To the same way, writing data at the latest communication shall be written to specified register address untill StopCondition enabled in case of the communication was continued by Restart(Repeated start)Condition.

Specific Register for Configuration

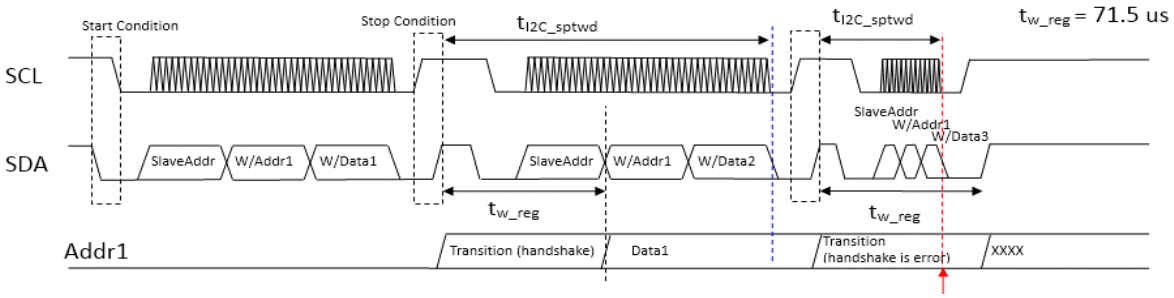
Addr	Symbol	Name	Description
15h	ISO	INT Source	Interrupt Source Setting
16h	FFCF	FIFO Config	FIFO mode, FIFO threshold
17h	SCF1	Sensor Config1	TAP, Mode, ODR

Interval time

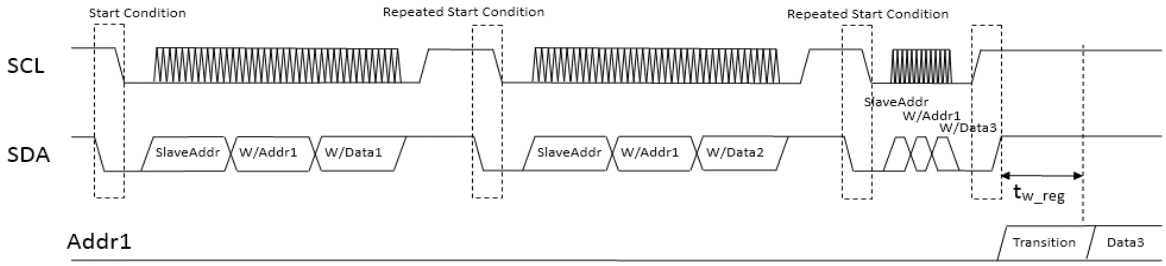
Parameter	Symbol	Condition	Characteristics			Units
			MIN	TYP	MAX	
Interval time from Stop Condition to Write Data of same address	t_{I2C_sptwd}	All Condition	71.5			us

INTERFACE SPECIFICATIONS I2C (Continued)

Register write constraints (Continued)



I^2C Specific Register Write Constraints



I^2C Repeated Start Condition Write to Same Register

Comminucation Frequency Constraints

- There is a possibility to lose the data under 1kHz for I2C,
  since next measurement data update is done during data reading.

Comminucation Frequency Constraints

I/F	ODR	Data Period	Constraints	Min Frequency
I^2C	100Hz	10ms	5 SCL < 10ms	0.5kHz
I^2C	200Hz	5ms	5 SCL < 5ms	1kHz

INTERFACE SPECIFICATIONS I2C (Continued)

I2C SLAVE INTERFACE

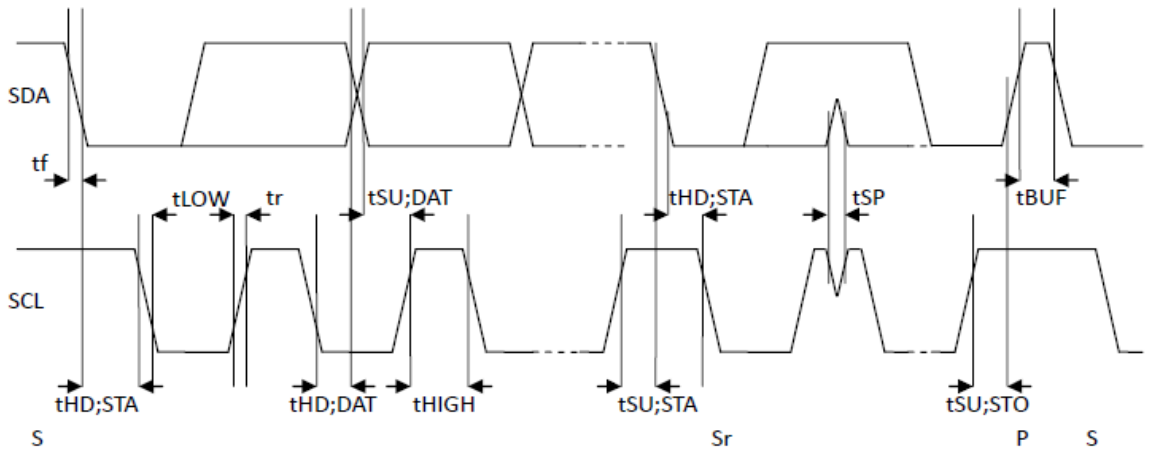
- Conformable to Philips I2C-Bus Specifications Version 2.1 and NXP UM10204 I2C-bus specification and user manual Rev.03-19 June 2007
- Slave address is SA0=0 : 0E(Hex), SA0=1 : 0F(Hex)
- Support Standard mode, Fast mode and Fast mode Plus.
- It is seemless change from Fast mode to High speed mode to use the master code (00001XXX)

I2C Characteristics

I2C Bus Timing1

Parameters	Symbol	Standard Mode		Fast mode		Fast mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold time (re)start condition	$t_{HD;STA}$	4.0	-	0.6	-	0.26	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	1.3	-	0.5	-	us
High period of the SCL clock	t_{HIGH}	4	-	0.6	-	0.26	-	us
Set-up time for (re)start condition	$t_{SU;STA}$	4.7	-	0.6	-	0.26	-	us
Data hold time	$t_{HD;DAT}$	0	-	0	-	0	-	us
Data set-up time	$t_{SU;DAT}$	250	-	100	-	50	-	ns
Rise time of SDA and SCL	t_r	600	1000	180	300	72	120	ns
Fall time of SDA and SCL	t_f	6.5	106.5	6.5	300	6.5	81.5	ns
Set-up time for stop condition	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	us
Bus free time between a stop and start condition	t_{BUF}	4.7	-	1.3	-	0.5	-	us
Capcacitive load for SDA/SCL	C_b	-	400	-	400	-	300	pF
Data valid time	$t_{VD;DAT}$	0.07	3.45	0.07	0.9	0.07	0.45	us
Data valid acknowledge time	$t_{VD;ACK}$	0.07	3.45	0.07	0.9	0.07	0.45	us
Noise margin at the low level	VnL	0.1*VDDIO	-	0.1*VDDIO	-	0.1*VDDIO	-	V
Noise margin at the high level	VnH	0.2*VDDIO	-	0.2*VDDIO	-	0.2*VDDIO	-	V
Hysteresis input voltage VDDIO < 2V	Vhys	0.1*VDDIO	-	0.1*VDDIO	-	0.1*VDDIO	-	V
Noise suppression pulse width	tsp	50	-	50	-	50	-	ns
I2C Glitch Suppression	I^2C_{GS}	150	200	150	200	150	200	mV

I2C Bus Timing



INTERFACE SPECIFICATIONS I2C (Continued)

I2C SLAVE INTERFACE (Continued)

- Data transfers follow the combined format with 7-bit addressing of I2C interface.
- Data is transferred with the most significant bit (MSB) first and little endian.
- Auto-increment of previous accessed register address is available when the internal register address is written during the first data byte. Data then can be transferred continuously.

Bus protocol definitions

S: Start condition
SAD+W: Slave Address + write bit
SAD+R: Slave Address + read bit
SAD+R/W:Slave Address + read or write bit
SA: Slave Acknoledge
ADR: Register Address(2nd byte)
Sr: Repeat Start condition
A: (Master) Acknowledge
/A: (Master) Non-Acknowledge
DATA: Data(load)
P: Stop condition
M-code: Master code (00001XXX)

Read Formats

One Byte Read

Master	S	SAD+W		ADR		P
Slave			SA		SA	

Master	S	SAD+R			/A	P
Slave			SA	DATA		

One Byte Read with repeat start condition

Master	S	SAD+W		ADR		Sr	SAD+R			/A	P
Slave			SA		SA			SA	DATA		

Multiple Bytes Read

Master	S	SAD+W		ADR		P
Slave			SA		SA	

Master	S	SAD+R			A		A		/A	P	
Slave			SA	DATA		DATA		DATA			

Multiple Bytes Read with repeat start condition

Master	S	SAD+W		ADR		Sr	SAD+R			A
Slave			SA		SA			SA	DATA	

	A		A		/A	P
DATA		DATA		DATA		

I^2C Standard / Fast / Fast Mode plus read communication protocol

Write Format

One Byte Write

Master	S	SAD+W		ADR		DATA		P
Slave			SA		SA		SA	

Multiple Bytes Write

Master	S	SAD+W		ADR		DATA		DATA		P
Slave			SA		SA		SA		SA	

I^2C Standard / Fast / Fast Mode plus write communication protocol

REGISTER DESCRIPTIONS

Supplier ID Register

Address : 00h, "Supplier ID"

Addess	bit	Symbol	R/W	Init	Description
00h	7:0	SID	R	49h	Supplier ID from customer

Chip ID Register

Address : 01h, "Chip ID"

Addess	bit	Symbol	R/W	Init	Description
01h	7:0	CPID	R	18h	Chip ID from customer

Revision ID Register

Address : 02h, "Revision ID"

Addess	bit	Symbol	R/W	Init	Description
02h	7:0	RVID	R	01h	Revision ID from ALSPALPINE

Chip Config Register

Address : 11h, "Chip Config"(CCF)

Address	bit	Symbol	R/W	Init	Description
11h	7:5	RSV	R	0h	Reserved
	4	SPIM	R/W	SPIV	SPIModeSelection
	3:1	RSV	R	0h	Reserved
	0	SRST	R/W	0h	Software Reset 1 : Enable Reset 0 : Normal After Software Reset completed, automatically return 0.

Interrupt Config Register

Address : 14h, "Interrupt Config"(ICF)

Address	bit	Symbol	R/W	Init	Description
14h	7:3	RSV	R	00h	Reserved
	2	IMLP	R/W	0b	Intterupt Mode 1 : Latched Mode 0 : Pulsed Mode
	1	IPPO	R/W	1b	Drive Circuit of INT pin 1 : Push-Pull 0 : Open drain
	0	IPOL	R/W	1b	Interrupt Polarity 1 : Active High 0 : Active Low

REGISTER DESCRIPTIONS (Continued)

Interrupt Source Register

Address : 15h, "Interrupt Source"(ISO)

Address	bit	Symbol	R/W	Init	Description
15h	7:4	RSV	R	00h	Reserved
	3	DRDY	R/W	0b	Interrupt Enable for DRDY signal 1 : DRDY Enable 0 : DRDY Disable
	2	FTHS	R/W	0b	Interrupt Enable for FIFO Threshold 1 : FIFO Threshlod Enable 0 : FIFO Threshold Disable
	1	FFUL	R/W	0b	Interrupt Enable for FIFO FULL 1 : FIFO Full Enable 0 : FIFO Full Disable
	0	RSV	R	0b	Reserved

FIFO Config Register

Address: 16h, "FIFO Config"(FFCF)

Address	bit	Symbol	R/W	Init	Description
16h	7:6	FFMD	R/W	00b	FIFO Mode Control 00 : Bypass Mode 01 : Stream-to-FIFO Mode 10 : STOP-on-FULL Mode 11 : Bypass Mode
	5:0	FFTH	R/W	00h	FIFO Threshold 0x00 : Disable the FIFO threshold 0x3F : 63 frames

Sensor Config Register

Address : 17h, "Sensor Config"(SCF1)

Addess	bit	Symbol	R/W	Init	Description
17h	7	TDIS	R/W	0b	TEMP measurement disable 1: TEMP measurement disable 0: TEMP measurement is performed with CMM or OSM
	6	RES	R	0b	Resolution Change 1: 0.0375uT/LSB output Range is +-1.2mT 0: 0.075uT/LSB output Range is +-2.4mT
	5:4	TAP	R/W	10b	Measurement TAP option for CMM 00: 6bit TAP(Ultra Low Power setting) 01: 7bit TAP(Low Power setting) 10: 8bit TAP(Default setting) 11: 9bit TAP(Low Noise setting)
	3:2	MODE	R/W	00b	Measurement Mode Selection 00: Standby Mode 01: Continuous Measurement Mode(CMM) 10: Reserve 11: One-Shot Mode(OSM)
	1:0	ODR	R/W	00b	Output Data Rate 00: 200Hz 01: 100Hz 10: 50Hz 11: 10Hz

REGISTER DESCRIPTIONS (Continued)

TEMP Measurement Register

Address : 1Dh to 1Eh, "TEMP Measurement Data"(TEMP)

Address	bit	Symbol	R/W	Init	Description
1Dh	7:0	TEMP	R	7Fh	TEMP data LSB TEMP[7:0]
1Eh	7:0	TEMP	R	7Fh	TEMP data MSB TEMP[15:8] TEMP[15:0] 16bit signed value -40 degC : FB00h (-1280d) 25 degC : 0320h (800d) 85 degC : 0AA0h (2720d) TEMP internal initial value is 0320h (800d) = 25 degC for compensation. TEMP sensor slope is 32LSB/degC.

Address : 1Fh to 24h, "Magnetometer Measurement Data"(MAGX, MAGY, MAGZ)

GMR Measurement Output Register

- 16bit integer and 7FFFh (+32767d) ～ 8000h (-32768d).

Address	bit	Symbol	R/W	Init	Description
1Fh	7:0	MAGX	R	7Fh	Magnetometer X axis measreuemnt data LSB MAGX[7:0]
20h	7:0	MAGX	R	7Fh	Magnetometer X axis measreuemnt data MSB MAGX[15:8]
21h	7:0	MAGY	R	7Fh	Magnetometer Y axis measreuemnt data LSB MAGY[7:0]
22h	7:0	MAGY	R	7Fh	Magnetometer Y axis measreuemnt data MSB MAGY[15:8]
23h	7:0	MAGZ	R	7Fh	Magnetometer Z axis measreuemnt data LSB MAGZ[7:0]
24h	7:0	MAGZ	R	7Fh	Magnetometer Z axis measreuemnt data MSB MAGZ[15:8]

Interrupt Status Register

Address : 25h, "Interrupt Status"(ISTA)

Address	bit	Symbol	R/W	Init	Description
25h	7:5	RSV	R	0b	Reserved
	4	POR	R	0b	POR complete and Software reset completed indicator 1 : completed 0 : not complete
	3	DRDY	R	0b	Data Ready indicator 1 : Active 0 : Inactive
	2	FTHS	R	0b	FIFO Threshold indicator FCNT >= FTHS 1 : Active 0 : Inactive
	1	FFUL	R	0b	FIFO Full indicator FCNT = 64 1 : Active 0 : Inactive
	0	RSV	R	0b	Reserved

Note) The indicators are clear on read register

REGISTER DESCRIPTIONS (Continued)

FIFO Register

Address : 26h, "FIFO Count"(FCNT)

Address	bit	Symbol	R/W	Init	Description
26h	7:0	FCNT	R	00h	The count number of FIFO data store 00h : empty 3Fh : 63 frames 40h : 64 frames (FIFO full)

Address : 27h, "FIFO Data Register"(FOUT)

Address	Bit	Symbol	R/W	Init	Description
27h	7:0	FOUT	R	7Fh	FIFO data output register address FIFO frame is composed 16 byte

Frame structure

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Reserved								Temp		Magnetometer					
-								TEMP		MAGX		MAGY		MAGZ	

Byte	Bit	Symbol	R/W	Init	Description
1	7:0	REV	R	-	Reserved byte
2	7:0	REV	R	-	Reserved byte
3	7:0	REV	R	-	Reserved byte
4	7:0	REV	R	-	Reserved byte
5	7:0	REV	R	-	Reserved byte
6	7:0	REV	R	-	Reserved byte
7	7:0	REV	R	-	Reserved byte
8	7:0	TEMP	R	7Fh	Temp measurement data low byte, if empty, output is 7Fh
9	15:8	TEMP	R	7Fh	Temp measurement data high byte, if empty, output is 7Fh
10	7:0	MAGX	R	7Fh	Mag X measurement data low byte, if empty, output is 7Fh
11	15:8	MAGX	R	7Fh	Mag X measurement data high byte, if empty, output is 7Fh
12	7:0	MAGY	R	7Fh	Mag Y measurement data low byte, if empty, output is 7Fh
13	15:8	MAGY	R	7Fh	Mag Y measurement data high byte, if empty, output is 7Fh
14	7:0	MAGZ	R	7Fh	Mag Z Measurement data low byte, if empty, output is 7Fh
15	15:8	MAGZ	R	7Fh	Mag Z measurement data high byte, if empty, output is 7Fh

REGISTER DESCRIPTIONS (Continued)

Sensor Action Register

'Address : 28h, "Sensor Action"(SACT)

Address	bit	Symbol	R/W	Init	Description
28h	7:2	RSV	R	00h	Reserved
	1	MES	R/W	0b	Magnetometer measurement. This function is available only One-Shot Mode. 1 : Performe Magnetmeter measurement. After measurement, this bit is returned 0 automatically. 0 : No action
	0	TMES	R/W	0b	TEMP measurement. This function is available only One-Shot Mode. 1 : Performe Temperature measurement. After measurement, this bit is returned 0 automatically. 0 : No action

REGISTER DEFINITIONS

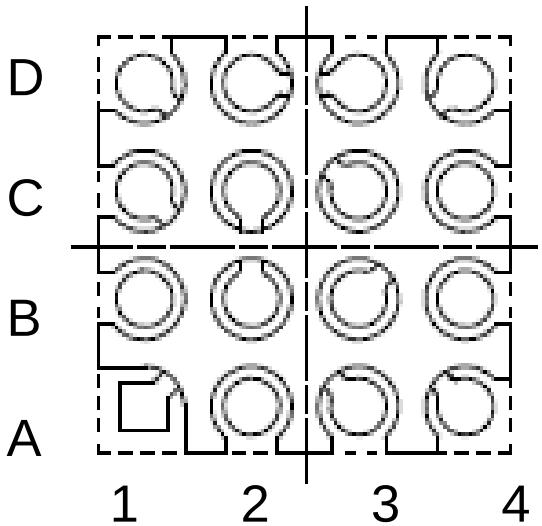
- Register addresses and definitions are as follows.
- Sensor output values are signed integer (2's compliment) presentation and little Endian order.

Address	R/W	Full Name	Symbol	Bit Map								Init
				D7	D6	D5	D4	D3	D2	D1	D0	
00h	R	Supplier ID	SID	0	1	0	0	1	0	0	1	49h
01h	R	Chip ID	CPID	0	0	0	1	1	0	0	0	18h
02h	R	Revision ID	RVID	0	0	0	0	0	0	0	1	01h
03h ~ 10h	R	Reserved										-
11h	RW	Chip Config	CCF				SPIM				SRST	00h
12h	R	Reserved										-
13h	R											
14h	RW	INT Config	ICF						IMLP	IPPO	IPOL	03h
15h	RW	INT Source	ISO					DRDY	FTHS	FFUL		00h
16h	RW	SFIFO Config	FFCF	FFMD[1:0]		[5:0]FFTH						00h
17h	RW	Sensor Config1	SCF1	TDIS	RES	TAP[1:0]		MODE[1:0]		ODR[1:0]		00h
18h	R	Reserved										-
19h	R											
1Ah	R	Reserved Config1	RRG1									00h
1Bh	R	Reserved Config2	RRG2									00h
1Ch	R	Reserved Config3	RRG3									00h
1Dh	R	Temp Data LSB	TEMP	TEMP[7:0]								7Fh
1Eh	R	Temp Data MSB	TEMP	TEMP[15:8]								7Fh
1Fh	R	Mag X LSB	MAGX	MAGX[7:0]								7Fh
20h	R	Mag X MSB	MAGX	MAGX[15:8]								7Fh
21h	R	Mag Y LSB	MAGY	MAGY[7:0]								7Fh
22h	R	Mag Y MSB	MAGY	MAGY[15:8]								7Fh
23h	R	Mag Z LSB	MAGZ	MAGZ[7:0]								7Fh
24h	R	Mag Z MSB	MAGZ	MAGZ[15:8]								7Fh
25h	R	INT Status	ISTA				POR	DRDY	FTHS	FFUL		00h
26h	R	FIFO Count	FCNT		FCNT[6:0]							00h
27h	R	FIFO Data Reg	FOUT	FIFO output port								7Fh
28h	RW	Sensor Action	SACT							MES	TMES	00h

PIN CONFIGURATION

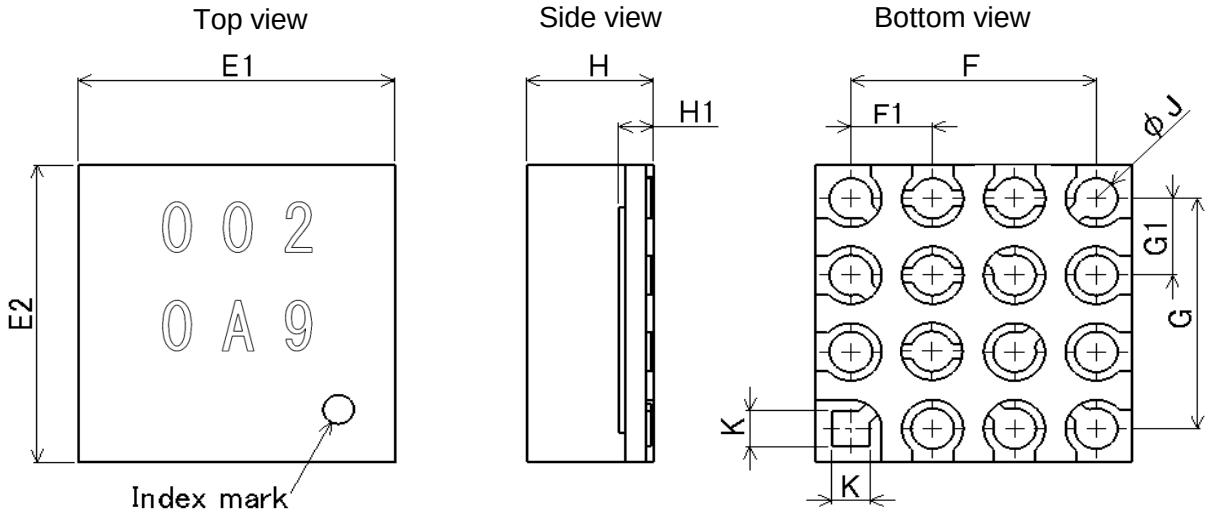
Pin	Symbol	Type	Description
A1	INT	Output, CMOS	Interrupt or Data Ready Selectable push-pull / open-drain open-drain state is implemented pull-up*
A2	(CSB)	(Input, CMOS)	(chip Select)
A3	SCL	Input, CMOS	I2C Serial Clock (SCL)
A4	SDA	Input/Output	I2C Serial Data (SDA)
B1	TEST	-	Factory use only Recommend GND connect
B2	NC	-	Non connect Connect GND or Floating is OK.
B3	TEST	-	Factory use only Recommend GND connect
B4	SA0	Input/Output, CMOS	I2C Slave Address
C1	GND	Power	Ground
C2	NC	-	Non connect Connect GND or Floating is OK.
C3	TRG	Input, CMOS	External Trigger Recommend GND connect
C4	AVDD	Power	Power supply
D1	TEST	-	Factory use only Only Floating
D2	NC	-	Non connect Connect GND or Floating is OK.
D3	NC	-	Non connect Connect GND or Floating is OK.
D4	VDDIO	Power	Power supply for I/O

Bottom view



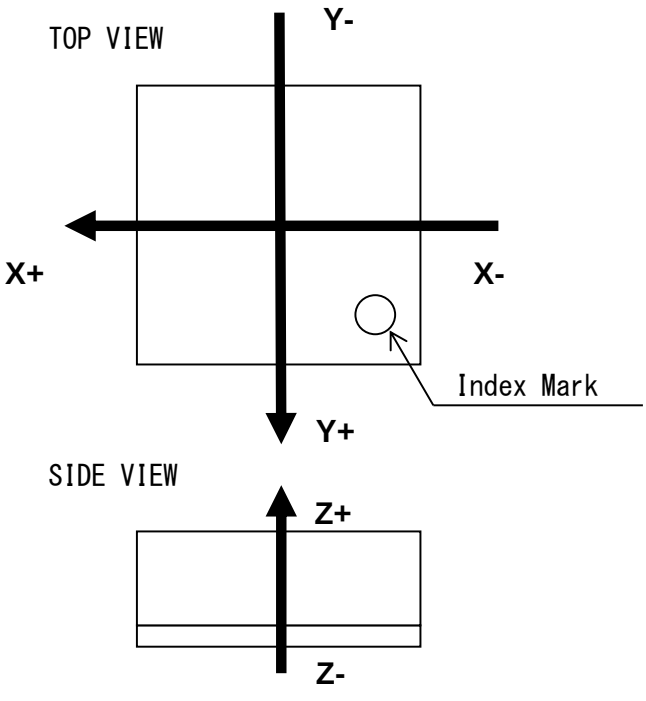
PACKAGE DIMENSIONS

Dimension in millimeters			unit: mm
Ref	Min.	Nom.	Max.
E1	1.50	1.55	1.60
E2	1.50	1.55	1.60
F	1.15	1.2	1.25
F1	0.35	0.4	0.45
G	1.15	1.2	1.25
G1	0.35	0.4	0.45
H	0.6	0.62	0.64
H1	0.13	0.16	0.19
J	0.185	0.21	0.235
K	0.161	0.186	0.211



PACKAGE DIRECTIONS

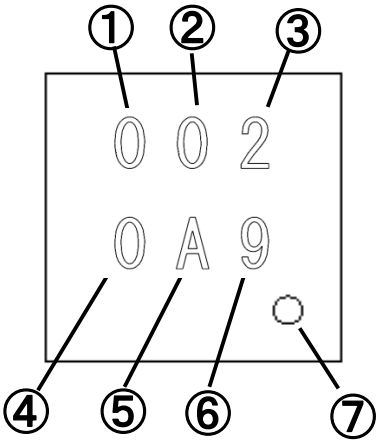
- X, Y, Z presents measurement directions of 3 axis sensor.
- Output value of each axis is positive when turned toward magnetic north.



Marking Specifications

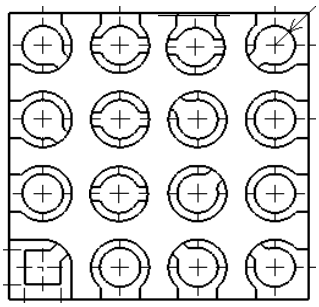
Front

top view



Back side

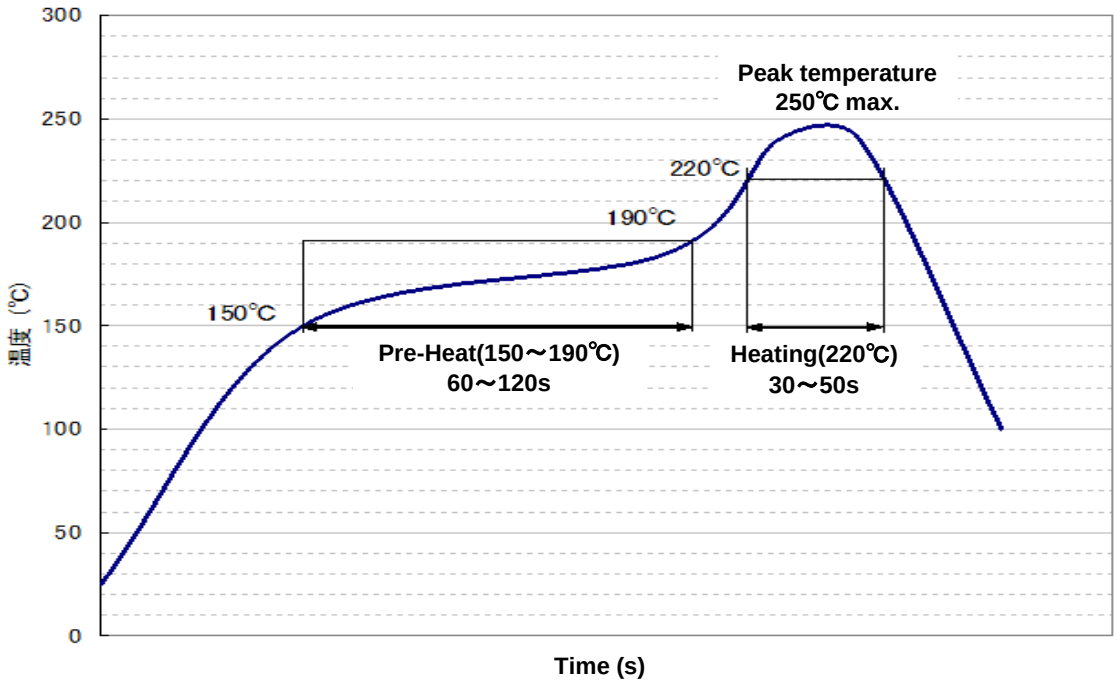
Bottom view



No.	Item	Indication content
① - ④	PWB No.	0 - 9, A - Z
⑤	Production month	1 - 9, A, B, C
⑥	Production site	9
⑦	1 Pin mark	●

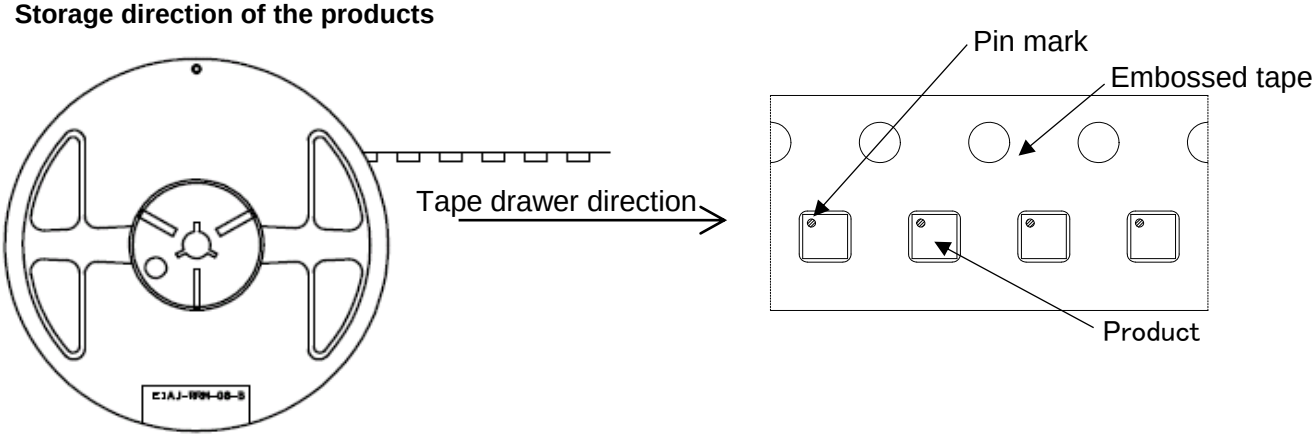
RECOMMENDED SOLDERING CONDITIONS

-The N_2 reflow is acceptable.
-Under the following conditions, the frequency of reflow soldering should be within two times.

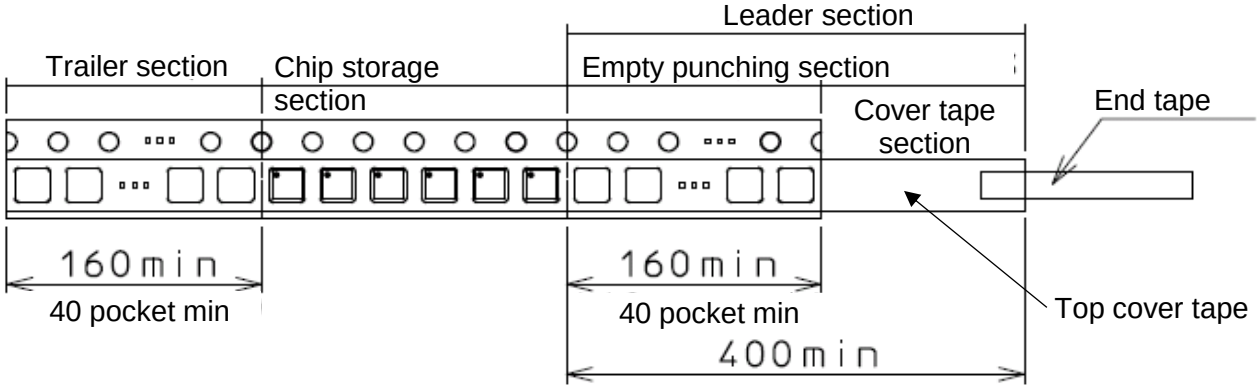


REEL AND TAPE

Storage direction of the products



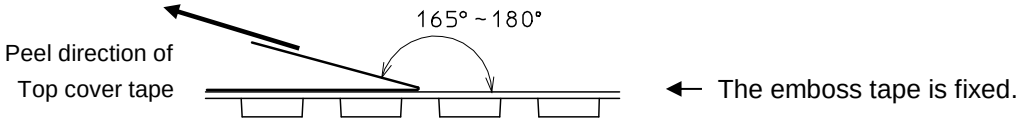
Taping



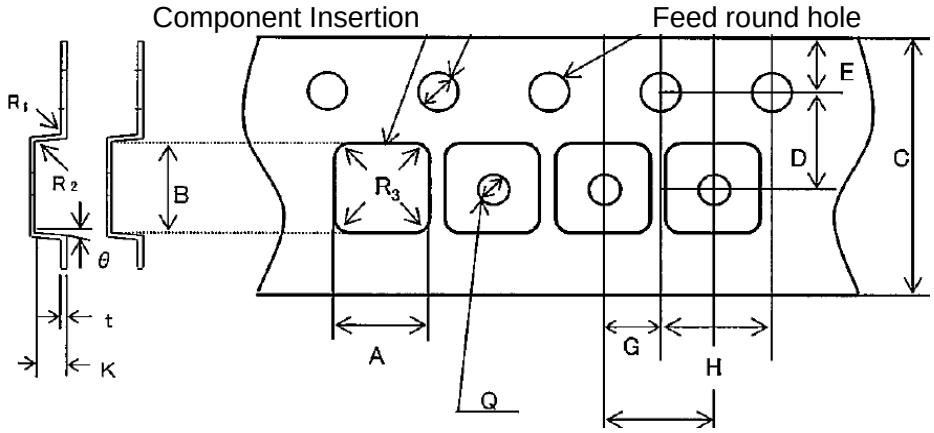
REEL AND TAPE (Continued)

Peel strength

- Peel strength of cover tape shall be 0.1N(10g)～0.7N(70g) for 300mm/min.



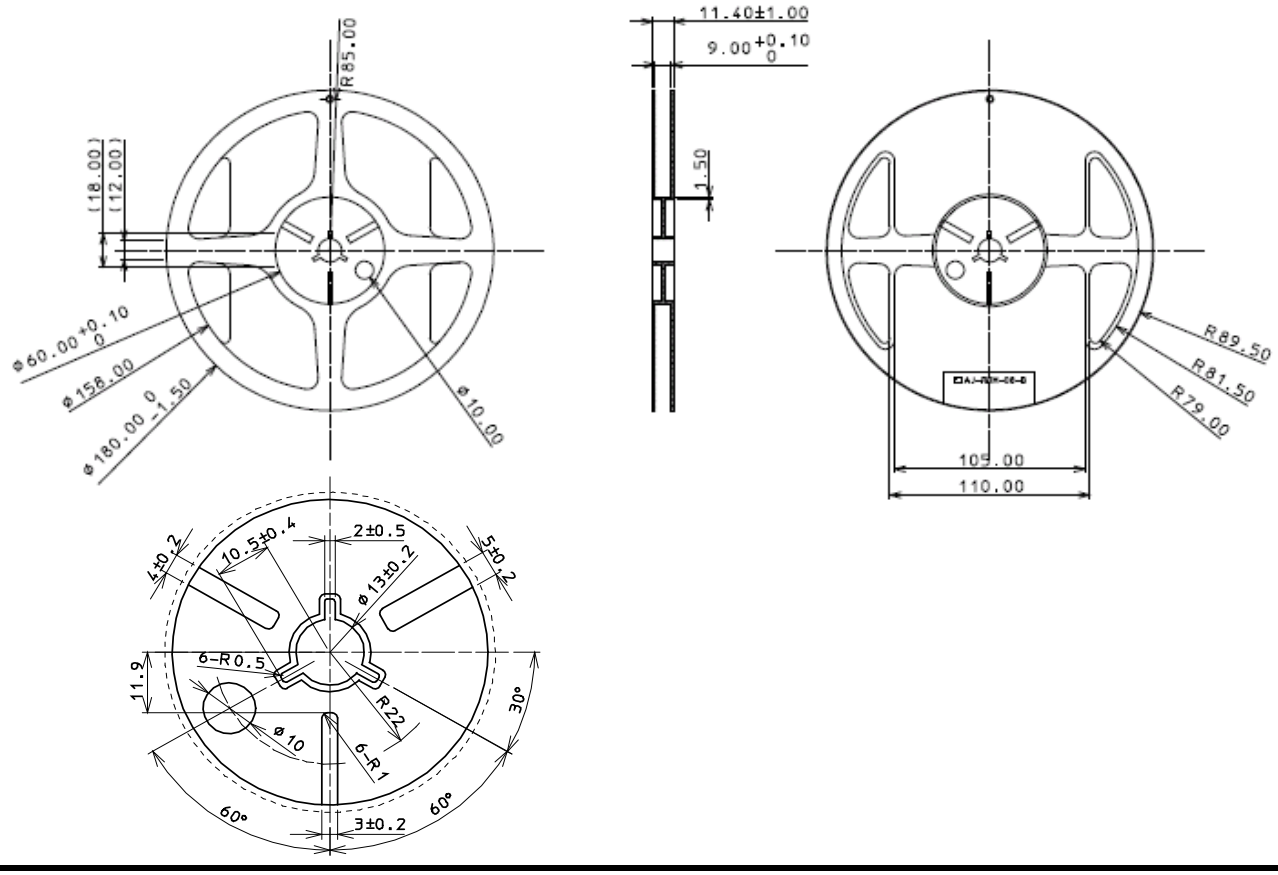
Emboss Tape Dimensions (Unit mm)



Symbol	A	B	C	D	E	F	G	H	J	K	Q	t
Dimensions	1.9±0.1	1.9±0.1	8.0±0.2	3.5±0.05	1.75±0.1	4.0±0.1	2.0±0.05	4.0±0.1	1.5 $^{+0.1}_{0}$	0.75±0.05	0.50±0.05	0.20±0.05

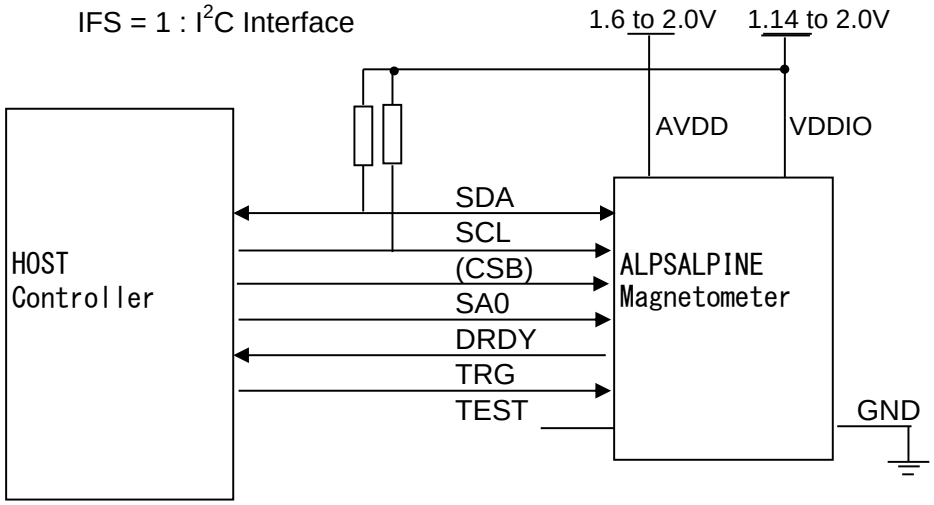
R_1	R_2	R_3	θ
0.3MAX	0.3MAX	0.3MAX	3° MAX

Reel Dimensions (Unit : mm)

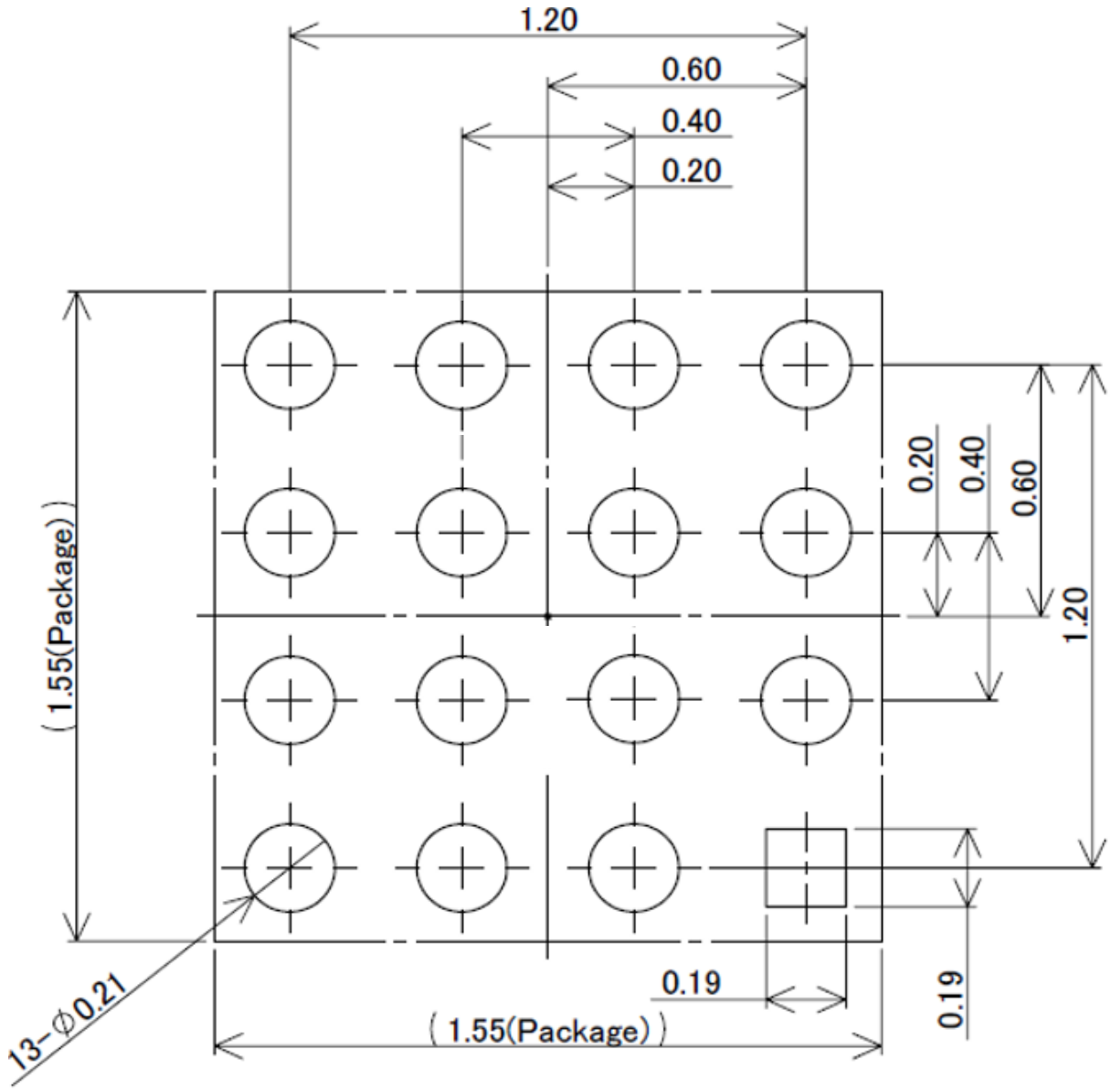


CONNECTION EXAMPLE

I2C Interface connection block diagram



RECOMMENDED LAND PATTERN



Asking that exports this product

1. For the export of products which are controlled items subject to foreign and domestic export laws and regulations, you must obtain approval and/or follow the formalities of such laws and regulations.

2. Products must not be used for military and/or antisocial purposes such as terrorism, and shall not be supplied to any party intending to use the products for such purposes.

3. Unless provided otherwise, the products have been designed and manufactured for application to equipment and devices which are sold to end-users in the market, such as AV (audio visual) equipment, home electric equipment, office and commercial electronic equipment, information and communication equipment or amusement equipment. The products are not intended for use in, and must not be used for, any application of nuclear equipment, driving control equipment for aerospace or any other unauthorized use.
   With the exception of the above mentioned banned applications, for applications involving high levels of safety and liability such as medical equipment, burglar alarm equipment, disaster prevention equipment and undersea equipment, please contact an Alps Alpine sales representative and/or evaluate the total system on the applicability. Also, implement a fail-safe design, protection circuit, redundant circuit, malfunction protection and/or fire protection into the complete system for safety and reliability of the total system.

4. Before using products which were not specifically designed for use in automotive applications, please contact an Alps Alpine sales representative.